

**ASSIGNMENT 5**

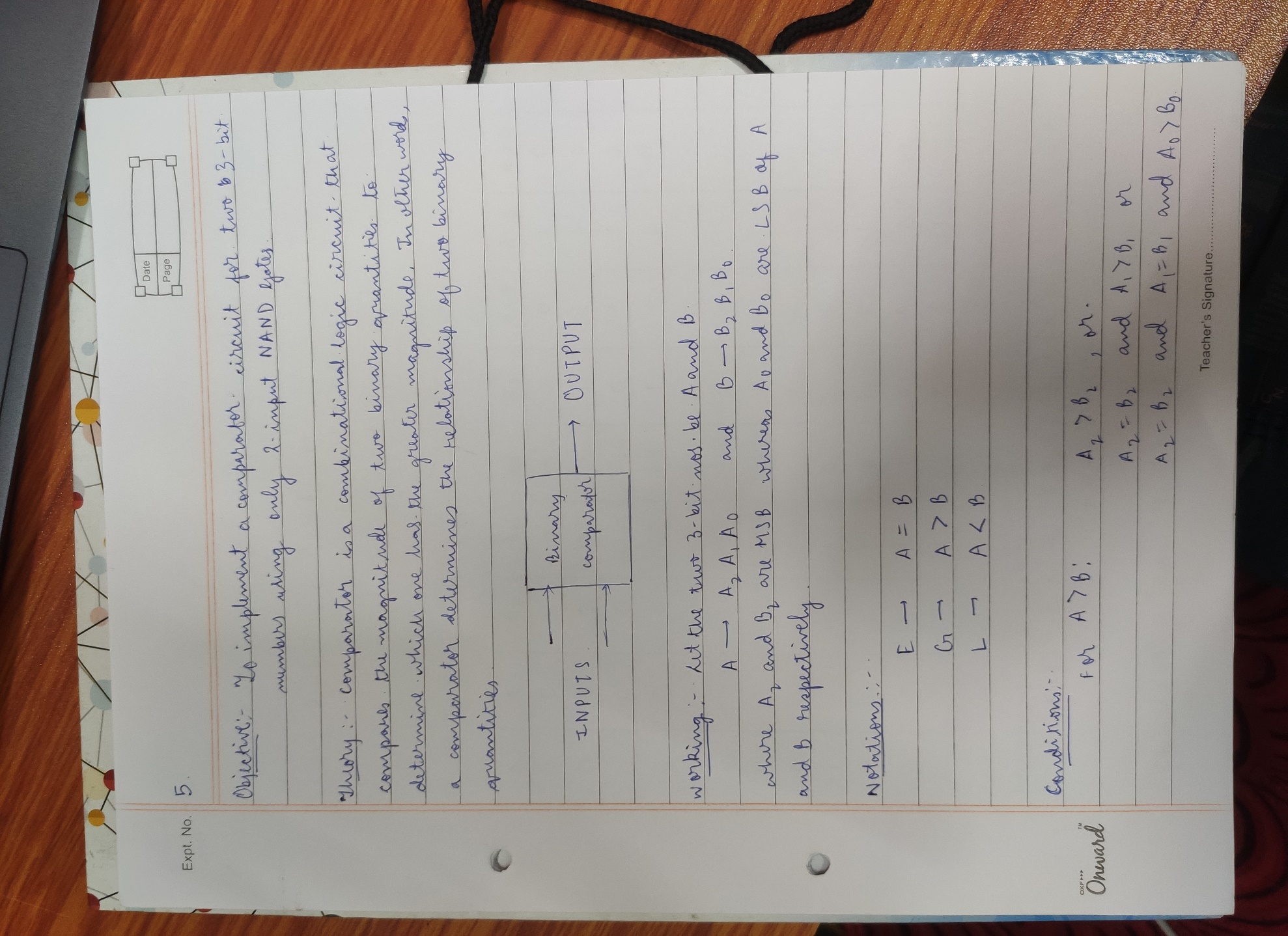
[Design of a combinational logic circuit for **3-BIT COMPARATOR** using 2 input NAND GATES]

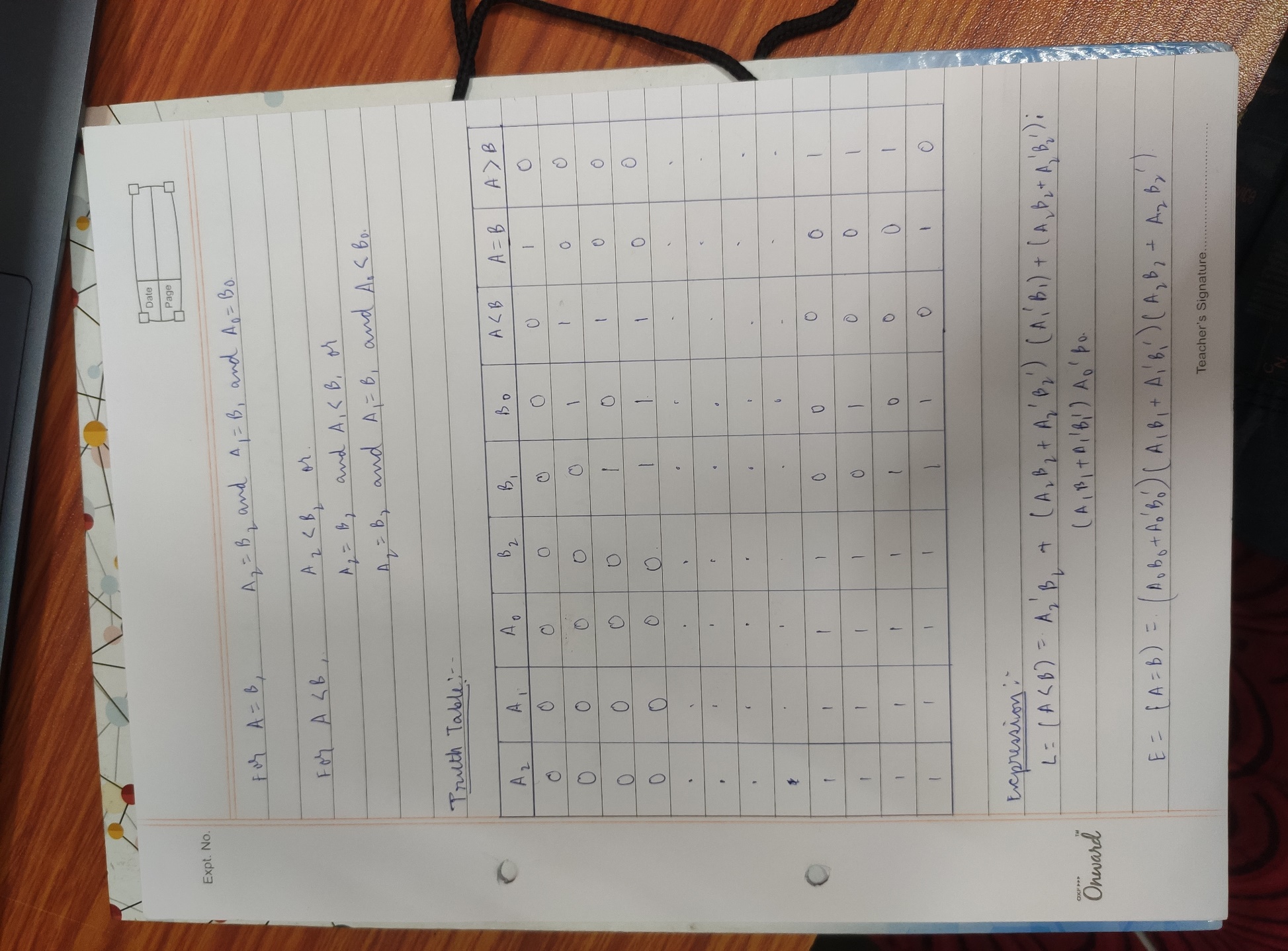


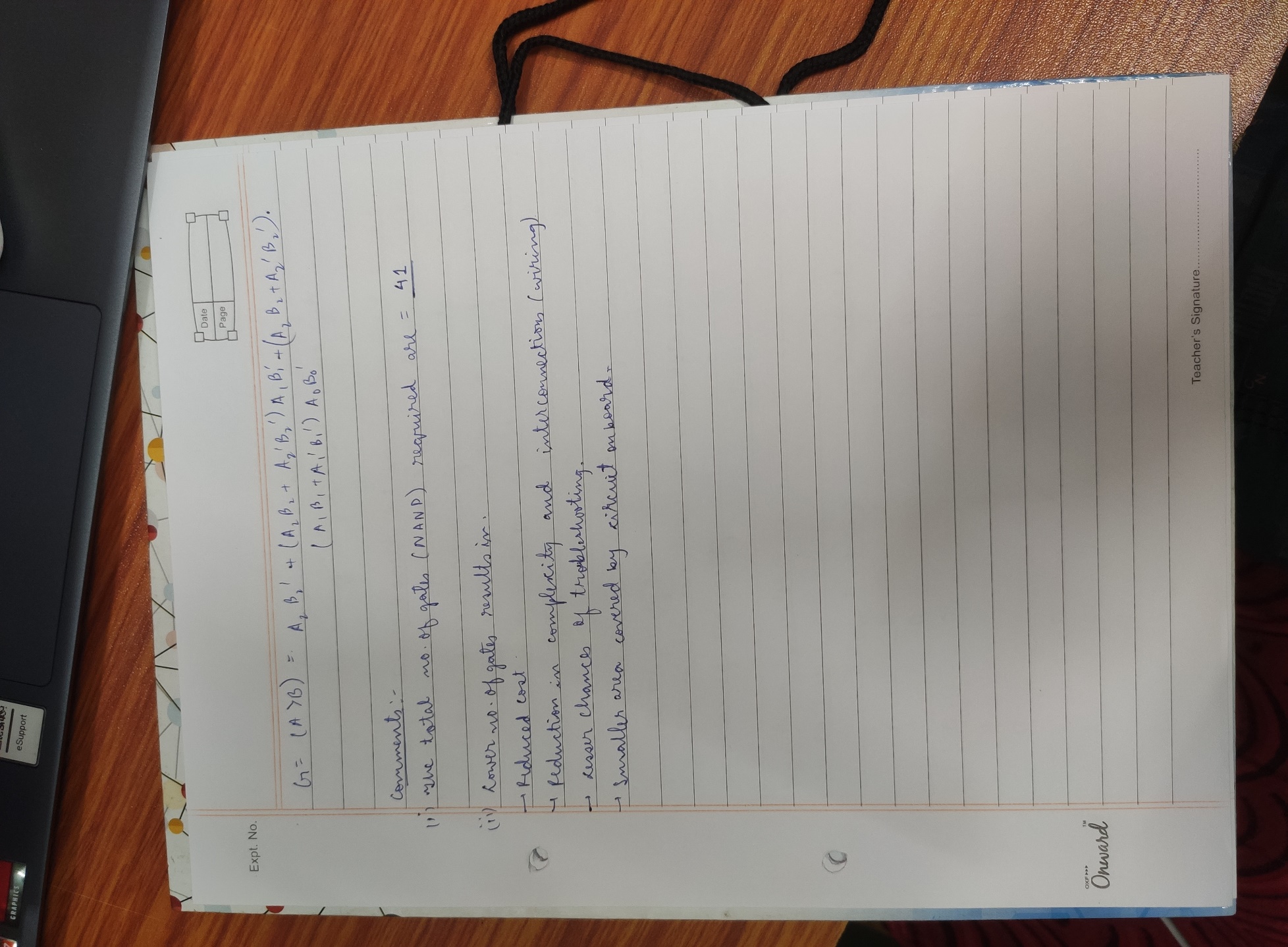
**NAME: ROHIT SADHU**

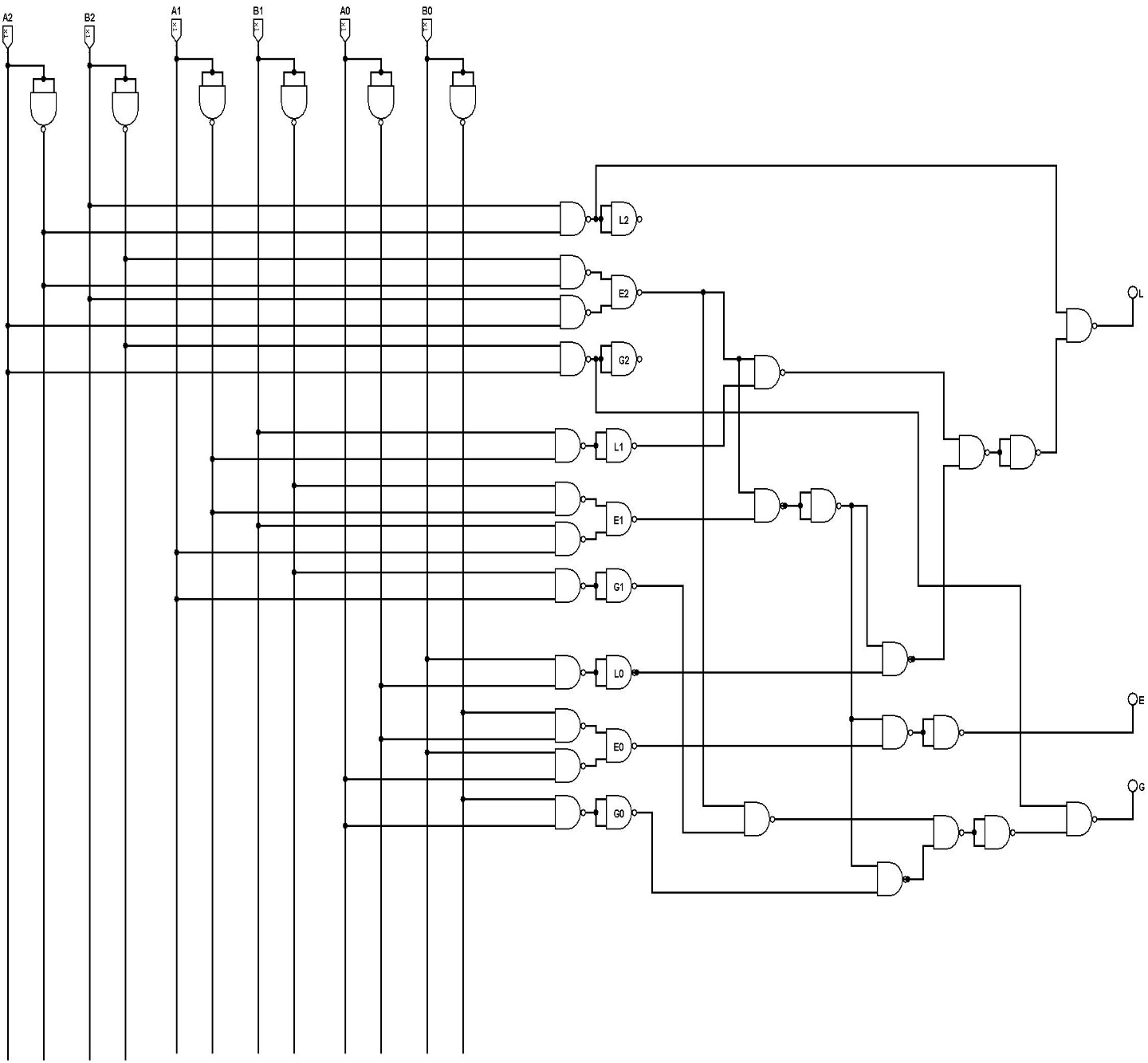
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**CIRCUIT DIAGRAM:**